First-In First-Out Memory System With Single Bit Collision Detection

ABSTRACT OF THE DISCLOSURE

[0041] An electronic device (10). The device comprises a memory structure (12) structure comprising an integer M of word storage locations. The device further comprises a shift register (SR_{RD}; SR_{WT}) for storing a sequence of bits. The sequence in the shift register comprises a number of bits equal to a ratio of $1/R_1$ times the integer M. The device further comprises circuitry (16) for providing a clock cycle to the shift register for selected data operations with respect to any of the word storage locations. The selected data operations are a data read or a data write. In response to each clock cycle, received from the circuitry for providing the clock cycle, the shift register shifts the sequence. Further, one bit in the sequence corresponds to an indication of one of the memory word storage locations from which a word will be read or into which a word will be written.